CLAIMS

What is claimed:

1. An integrated circuit (IC) device, comprising:

memory controller logic to generate address and command information for accessing a memory device;

a plurality of driver circuits on-chip with said memory controller logic;

a plurality of first signal pads on-chip with said memory controller logic, the plurality of driver circuits having outputs that are coupled to the plurality of signal pads, respectively; and

on-chip logic, coupled between the plurality of driver circuits and the controller logic, to a) transmit, at speed, address and command information generated by the controller logic, using the plurality of driver circuits and in a normal mode of operation for the IC device and b) transmit, at speed, test symbols, using the plurality of driver circuits and in a test mode of operation for the IC device during which a chip-to-chip connection between the IC device and another device is tested.

2. The IC device of claim 1 further comprising:

a plurality of second signal pads;

a plurality of receiver circuits whose inputs are coupled to the plurality of second signal pads, respectively; and

further logic coupled between the plurality of receiver circuits and the controller logic to a) forward data, received by the plurality of receiver circuits, to the controller logic in said normal mode of operation for the IC device and b) determine error in test symbols received by the plurality of receiver circuits in a test mode of operation for the IC device during which a chip-to-chip connection between the IC device and another device is tested.

3. The IC device of claim 1 further comprising:

a test access port coupled to the logic to transfer information regarding the determined error out of the IC device.

4. The IC device of claim 3 wherein the logic has boundary scan chain capability, to read test control and pattern information and write said error information.

5. A memory integrated circuit (IC) module, comprising:

a carrier substrate;

a plurality of first and second signal connection points being installed on the substrate;

a plurality of memory devices installed on the substrate, each of which has a separate memory core array and separate address decoder logic; and

a memory buffer installed on the substrate and communicatively coupled between the plurality of first and second signal connection points and the plurality of memory devices,

the buffer having a plurality of driver circuits whose outputs are coupled to the plurality of first signal connection points, respectively, and logic to a) forward read data, provided by the plurality of memory devices, at speed using the plurality of drivers in a normal mode of operation for the module and b) determine error in test symbols received from outside the module at speed using the plurality of second signal connection points in a test mode of operation for the module during which a chip-to-chip connection between the module and another device is tested.

6. The module of claim 5 wherein the carrier substrate is a printed wiring board and the plurality of memory devices are dynamic random access memory (DRAM) devices.

7. The module of claim 5 further comprising:

a plurality of third and fourth signal connection points being installed on the substrate; and

wherein the buffer device includes a further plurality of driver circuits whose outputs are coupled to the plurality of third signal connection points, respectively, and further logic to a) forward address and command information, that has been received from outside the module, at speed using the further plurality of driver circuits and b) determine error in test symbols, that have been received from outside the module at speed via the plurality of fourth signal connection points, in a test mode of operation for the module

during which a chip-to-chip connection between the module and another device is tested.

8. The module of claim 7 wherein the buffer device is to decode local memory command, address and data, received at speed via the plurality of second signal connection points, and send them to some of the plurality of memory devices.

9. A system of integrated circuit (IC) devices, comprising:

a carrier substrate;

a host IC device having memory controller logic and being installed on the substrate,

the host IC device having built-in self test (BIST) generator logic coupled between a plurality of driver circuits and the memory controller logic, to a) transmit, at speed, address and command information generated by the controller logic, using the plurality of driver circuits in a normal mode of operation for the IC device and b) transmit, at speed, test symbols, using the plurality of driver circuits in a test mode of operation for the IC device during which an interconnect between the IC device and another device is tested,

the host IC device having BIST checker logic coupled between a plurality of receiver circuits and the memory controller logic, to a) forward data, received by the plurality of receiver circuits, to the memory controller logic in said normal mode of operation for the IC device and b) determine error in test symbols received by the plurality of receiver circuits in a test mode of operation for the IC device during which an interconnect between the IC device and another device is tested; and

a first main memory module being installed on the substrate to communicate with the host IC device,

the first module having a memory buffer circuit with repeater capability to a) forward address and command information from the memory controller logic to a second main memory module, and b) forward read data from the second main memory module to the memory controller logic,

the first module having first BIST checker logic to determine error in the test symbols transmitted by the BIST generator logic of the host IC device.

10. The system of claim 9 further comprising the second main memory module installed on the substrate to communicate with the host IC device through the first main memory module,

the second module to re-transmit the test symbols transmitted by the host IC device and forwarded by the first module, back to the first module.

11. The system of claim 10 wherein the first module further comprises second BIST checker logic to determine error in the re-transmitted test symbols received from the second module.

12. The system of claim 9 wherein the host IC device is a processor device that includes a processor core coupled to the memory controller logic to access the main memory modules.

13. The system of claim 9 wherein the host IC device is a system chipset device that a processor of the system uses to access the main memory modules and computer system peripherals.

14. A method for testing a chip-to-chip connection in a computer system, comprising:

transmitting test symbols from a host integrated circuit (IC) device that is installed in a computer system, over a first outbound chip-to-chip communications connection of the system normally used by the host IC device to send address and command information at speed to access an installed main memory subsystem of the system, in a test mode of operation for the host IC device during which the first outbound connection is being tested, wherein the test symbols are transmitted at speed; and

receiving the test symbols and then checking them against a test symbol pattern stored in a first memory module of the subsystem.

15. The method of claim 14 further comprising:

looping the received test symbols in the first module back to the host IC device over a first inbound chip-to-chip communications connection of the system normally used by the first module to send read data at speed to the host IC device, in a test mode of operation for the host IC device during which the

first inbound connection is being tested, wherein the received test symbols are looped back at speed; and

receiving the looped back test symbols and then checking them against a test symbol pattern stored in the host IC device.

16. The method of claim 14 further comprising:

re-transmitting the received test symbols from the first module, over a second outbound chip-to-chip communications connection of the system normally used by the first module to send memory address and command information at speed to a second memory module of the subsystem, in a test mode of operation for the second module during which the second outbound connection is being tested, wherein the received test symbols are re-transmitted at speed; and

receiving the re-transmitted test symbols and then checking them against a test symbol pattern stored in the second module.

17. The method of claim 16 further comprising:

looping the received re-transmitted test symbols in the second module back to the host IC device over a first inbound chip-to-chip communications connection of the system normally used by the second module to send read data at speed to the host IC device, in a test mode of operation for the first module during which the first inbound connection is being tested, wherein the received re-transmitted test symbols are looped back at speed; and

receiving the looped back test symbols and checking them against a test symbol pattern stored in the first module.

18. The method of claim 17 further comprising:

re-transmitting the received, looped back test symbols from the first module, over a second inbound chip-to-chip communications connection of the system normally used by the first module to send read data at speed to the host IC device, in a test mode of operation for the host IC device during which the second inbound connection is being tested, wherein the received, looped back test symbols are re-transmitted at speed; and

receiving the re-transmitted, received, looped back test symbols and then checking them against a test symbol pattern stored in the host IC device.

19. A method for testing a memory module, comprising:

transmitting test symbols, generated in a memory buffer device that is installed in a memory module, from the memory buffer device over an outbound chip to chip communications connection of the module normally used by the module to forward memory address and command information at speed to another memory module of a main memory subsystem, wherein the test symbols are transmitted at speed during a test mode of operation for the module during which the module self-tests its interconnect;

looping the transmitted test symbols back to the memory buffer device over an inbound chip to chip communications connection of the module normally used by the module to send read data at speed to a host device; and

receiving the looped back test symbols in the memory buffer device and checking them using a test symbol pattern stored in the module.

20. The method of claim 19 further comprising storing error information obtained from said checking in the memory buffer device, and reading the error information out of the memory buffer device.

21. A method for testing a memory module, comprising:

transmitting test symbols, generated in a memory buffer device that is installed in a memory module, from the memory buffer device over an inbound chip to chip communications connection of the module normally used by the module to forward read data at speed to a host device for a main memory subsystem, wherein the test symbols are transmitted at speed during a test mode of operation for the module during which the module self-tests its interconnect;

looping the transmitted test symbols back to the memory buffer device over an outbound chip to chip communications connection of the module normally used by the module to receive memory address and command information at speed from the host device; and

receiving the looped back test symbols in the memory buffer device and checking them using a test symbol pattern stored in the module.